CLAIMS IN CURRENT FORM

1. (PREVIOUSLY PRESENTED) A method for reducing power consumption during background operations in a memory array with a plurality of sections comprising the steps of:

controlling said background operations in each of said plurality of sections of said memory array in response to one or more control signals, wherein said background operations can be enabled simultaneously in two or more of said plurality of sections independently of any other section; and

presenting said one or more control signals and one or more decoded address signals to one or more periphery array circuits of said plurality of sections.

2. (ORIGINAL) The method according to claim 1, wherein said background operations comprise a refresh operation.

3. (ORIGINAL) The method according to claim 1, wherein said plurality of sections comprise quadrants.

4. (ORIGINAL) The method according to claim 1, wherein said background operations comprise parity checking.

5. (ORIGINAL) The method according to claim 1, further comprising:

controlling, in response to said one or more control signals, an operation of said one or more periphery array circuits, wherein said periphery array circuits each comprise one or more circuits from the group consisting of sense amplifiers, column multiplexer circuits, equalization circuits, and wordline driver circuits.

6. (ORIGINAL) The method according to claim 1, further comprising:

generating one of said one or more control signals for each of said plurality of sections of said memory array.

7. (ORIGINAL) The method according to claim 1, wherein said one or more control signals are generated in response to an address signal.

8. (ORIGINAL) The method according to claim 1, further comprising:

generating said one or more control signals in response to a refresh enable signal.

9. (ORIGINAL) The method according to claim 8, further comprising generating a memory cell selection signal comprising a binary numerical representation configured such that a single bit

changes between successive numbers in response to said refresh enable signal.

10. (PREVIOUSLY PRESENTED) An apparatus comprising:

means for controlling a background operation in each of a plurality of sections of a memory array in response to one or more control signals, wherein said background operations can be enabled simultaneously in two or more of said plurality of sections independently of any other section; and

means for presenting said one or more control signals and one or more decoded address signals to one or more periphery array circuits of said plurality of sections.

11. (PREVIOUSLY PRESENTED) An apparatus comprising:

a memory array comprising a plurality of sections, wherein each of said sections comprises (i) a plurality of memory cells and (ii) periphery array circuitry configured to control access to said plurality of memory cells; and

a control circuit configured to present one or more control signals and one or more decoded address signals to said periphery array circuitry of said plurality of sections, wherein a background operation in each of said plurality of sections is controlled in response to said one or more control signals and said background operation can be enabled simultaneously in two or more of said plurality of sections independently of any other section.

12. (ORIGINAL) The apparatus according to claim 11, wherein said background operation comprises a refresh operation.

13. (ORIGINAL) The apparatus according to claim 11, wherein each of said one or more control signals is configured to control one or more array control signals of a corresponding section.

14. (ORIGINAL) The apparatus according to claim 11, wherein said periphery array circuitry comprises one or more sense amplifiers configured to sense a memory cell state in response to said one or more control signals and said one or more decoded address signals.

15. (ORIGINAL) The apparatus according to claim 11, wherein said periphery array circuitry is configured to generate one or more wordline signals in response to said one or more control signals and said one or more decoded address signals.

16. (ORIGINAL) The apparatus according to claim 11, wherein said periphery array circuitry comprises equalization circuitry configured to equalize one or more bitlines to a predetermined voltage potential in response to said one or more control signals and said one or more decoded address signals.

17. (ORIGINAL) The apparatus according to claim 11, wherein said periphery array circuitry comprises column multiplexing circuitry.

18. (ORIGINAL) The apparatus according to claim 11, wherein said one or more control signals are generated in response to an address signal.

19. (ORIGINAL) The apparatus according to claim 11, wherein each of said memory cells comprises a dynamic storage element.

20. (ORIGINAL) The apparatus according to claim 11, wherein said background operation comprises parity checking.

21. (ORIGINAL) The apparatus according to claim 11, wherein said one or more decoded address signals comprise one or more decoded row address signals and one or more decoded column address signals.

22. (ORIGINAL) The apparatus according to claim 11, wherein said periphery array circuitry of each of said plurality of sections is configured to control said plurality of memory cells of each of said plurality of sections in response to (i) said one or more control signals and (ii) said one or more decoded address signals.

23. (ORIGINAL) The apparatus according to claim 11, wherein said memory array comprises a plurality of blocks and each block of said plurality of blocks comprises two or more of said plurality of sections.

24. (ORIGINAL) The method according to claim 1, wherein said one or more decoded address signals comprise one or more decoded row address signals and one or more decoded column address signals.

25. (ORIGINAL) The method according to claim 1, wherein said background operations are enabled in response to a first state of said one or more control signals.

26. (ORIGINAL) The method according to claim 1, wherein said background operations are disabled in response to a first state of said one or more control signals.

27. (PREVIOUSLY PRESENTED) A method for reducing power consumption during parity checking in a memory array with a plurality of sections comprising the steps of:

controlling said parity checking in one or more of said plurality of sections of said memory array in response to one or more control signals; and

presenting said one or more control signals and one or more decoded address signals to one or more periphery array circuits of said one or more sections.

28. (PREVIOUSLY PRESENTED) A method for reducing power consumption during background operations in a memory array with a plurality of sections comprising the steps of:

controlling said background operations in one or more of said plurality of sections of said memory array in response to one or more control signals;

presenting said one or more control signals and one or more decoded address signals to one or more periphery array circuits of said one or more sections; and

generating a memory cell selection signal comprising a binary numerical representation configured such that a single bit changes between successive numbers in response to a refresh enable signal.

29. (PREVIOUSLY PRESENTED) The method according to claim 7, wherein said address signal is programmable.

30. (PREVIOUSLY PRESENTED) The apparatus according to claim 18, wherein said address signal is programmable.

31. (PREVIOUSLY PRESENTED) An apparatus comprising:

a memory array comprising a plurality of sections, wherein each of said sections comprises (i) a plurality of memory cells and (ii) periphery array circuitry configured to control access to said plurality of memory cells; and

a control circuit configured to present one or more control signals and one or more decoded address signals to said periphery array circuitry of said plurality of sections, wherein (a) a background operation in each of said plurality of sections (i) is controlled in response to said one or more control signals and (ii) can be enabled independently of any other section and (b) said control circuit comprises (i) an array control circuit configured to generate said one or more control signals in response to one or more block address signals and a refresh enable signal and (ii) a register configured to store said one or more block address signals.